Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S11 8	166	((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) same (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 08:24
S12 2	144	((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and "716"/$.ccls. and clock	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 08:44
S13 1	10	((redundant redundanc$3)near4(latch$3 register circuit gate cell macro)) near10 (reduc$3 eliminat$3 delet$3 remov$3 minimiz$3 optimiz$3)and (clock adj domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 08:54
S13 4	9	((redundant redundanc$3)same(latch$3 register circuit gate cell macro)) same (reduc$3 eliminat$3 delet$3 remov$3 minimiz$3 optimiz$3)same (domain)same clock	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 09:00
S13 8	281	(redundant redundanc$3)adj2(latch$3)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 09:16
S14 1	13	((redundant redundanc$3)near10(latch$3)) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 09:21
S15 7	7	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") same (reduc$3 eliminat$3 remov$3 combin$3) same (clock adj cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 15:55
S16 1	102	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") and (reduc$3 eliminat$3 remov$3 combin$3) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 16:00
S16 4	14	((redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop")) and (reduc$3 eliminat$3 remov$3 combin$3) and (logical adj function) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 16:03
S15 9	463	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") and (reduc$3 eliminat$3 remov$3 combin$3) and (clock adj cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 16:08

S169	13	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") and (reduc$3 eliminat$3 remov$3 combin$3) and (clock adj cycle) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 16:11
S173	45	retiming same (redundant redundancy)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/03 08:26
S175	26	retiming same (redundant redundancy)and latch$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/03 08:27
S179	492	(reduc$3 eliminat$3 remov$3) same (redundant redundancy)same (latch latches)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/03 08:29
S182	16	(reduc$3 eliminat$3 remov$3) same (redundant redundancy)same (latch latches gate circuit flip-flop "flip flop")and retiming and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/03 10:25
S181	236	(reduc$3 eliminat$3 remov$3) same (redundant redundancy)same (latch latches gate circuit flip-flop "flip flop")and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 10:20
S196	16	(reduc$3 eliminat$3 remov$3) same (redundant redundancy)same (latch latches gate circuit flip-flop "flip flop")and retiming and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 10:24
S210	54	((redundant redundanc$3)adj2(latch$3)) and ("physical design" layout)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 15:53
S213	11	((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and retiming and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:09
S218	29	((redundant redundanc$3)near5(latch$3 register)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and "716"/$. ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:13
S167	133	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") same (reduc$3 eliminat$3 remov$3 combin$3) and (clock adj cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:20

S221	47	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") same (reduc$3 eliminat$3 remov$3 combin$3) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:23
S223	77	"716"/$.ccls. and retiming	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:42
S230	47	layout and(redundan$3 adj2 latch$2)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:46
S233	31	layout and (redundan$3)same latch$2 same transition	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:48
S273	22	latch same transition same clock same period same combin$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 08:04
S276	12	redundant same (latch flip-flop register)same transition same (clock period) same combin$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 08:07
S282	2528	clock adj domain	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:28
S292	124	redundant and (latch$3 flip-flop register)and transition and (clock period) and combin$3 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:46
S293	82	redundant and (latch$3 flip-flop register)and transition and (clock period) and combin$3 and (clock adj domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:49
S294	10	redundant and (latch$3 flip-flop register)and transition and (clock period) and combin$3 and (clock adj domain) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:51
S298	3	redundant same (latch$3 flip-flop register)same transition and (clock adj domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:53
S301	115	(redundant redundancy)same (latch$3 flip-flop register)and (clock adj domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:57

S280	5861	latch same transition same (clock or period)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 10:35
S306	111	latch same transition same (clock or period) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 10:44
S281	5875	(group$3 or combin$3) adj6 latch	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 10:45
S308	507	S307 same transition	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 10:46
S318	51	layout same latch same optimiz$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 12:59
S320	9	layout and redundant same latch same optimiz$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 13:00
S327	20	(latch same transition) and (clock adj (period cycle))and (clock adj domain) and redundant	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 13:08
S332	22	(redund$3 adj2 latch$2) and transition and (clock adj cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 14:46
S338	62	(redund$3 adj2 (latch$2 flip-flop clocked-gate)) and transition and (clock cycle domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 15:46
S342	16	(redundant) adj2(latch$3 flip-flop gate circuit) and (clock adj domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 18:49
S365	24	(redundant redundancy) same (latch flip-flop) and transition and retiming and layout	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/09 12:28
S383	20	redundant same (latch flip-flop)and (minimiz$3 reduc$3 optimiz$3) and transition and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/09 14:21

S401	9	(latch flip-flop register) same (redundancy redundant) and clock adj2 transition and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/09 15:52
S418	3	(layout same optimiz$5) and redundan$4 adj (latch flip-flop register)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 08:58
S422	16	redundant adj2 (latch$3 flip-flop) and transition and (optimiz$3 compact$3)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 09:04
S442	54	physical same design same layout same latch	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 11:54
S449	79	design same layout same latch and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 12:00
S462	53	identify$3 same redundan$2 same latch	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2005/08/10 13:37
S471	1158	latch near4 collaps$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:23
S474	253939	S472 and S473	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:24
S473	593417	transition	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:24
S472	2427883	clock or period	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:24
S475	13	S474 and S471	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:37
S477	1	S474 and S471 and redundancy	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:38

S476	0	S474 and S471 and redundant	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:38
S487	83	logic same design same physical same layout same simulation	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/11 08:41
S502	24	latch same transition same layout same cycle	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/11 16:42
S505	61	latch same transition and layout and simulation and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/11 16:48
S578	128	selection same output same logic and "AND" and inverter and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/16 11:10
S583	3	selection adj logic same active adj output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/16 11:18
S585	32	selection adj logic same output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/16 11:21
S590	1	demultiplexor and inverter and ("AND" "and") and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/16 11:26
S591	16	selection adj logic and inverter and ("AND" "and") and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/16 11:30
S599	7	demultiplexor and logic and selection and gate and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:48
S611	825	latch near3 collaps$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:56
S614	2	S611 and S612	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:57

S615	594695	transition	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:58
S617	20356	S612 and S616	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:59
S616	20356	transition and clock adj (period cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:59
S612	58205	clock adj (period cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:59
S619	594695	transition	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:00
S618	2431651	clock or period	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:00
S621	8	S611 and S620	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:01
S620	254493	S618 and S619	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:01
S623	5	(latch flipflop FF ff register) same (select$3 multiplex$3 demultiplex$3 mux$3 demux$3) same (non-active nonactive inactive passiv$5) near5 output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:30
S625	18	(latch flipflop FF ff register) same (select$3 multiplex$3 demultiplex$3 mux$3 demux$3 de-mux$3) same (non-active nonactive inactive passiv$5 off non-operat$3 non-operatable nonoperat$3 nonoperatable inoperat$3 inoperatable) near5 output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:49
S622	572	(latch flipflop FF ff register) same (select$3 multiplex$3 demultiplex$3 mux$3 demux$3) same (non-active nonactive inactive passiv$5) near5 output	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 18:58

S624	18	(latch flipflop FF ff register) same (select$3 multiplex$3 demultiplex$3 mux$3 demux$3) same (non-active nonactive inactive passiv$5 off non-operat$3 non-operatable nonoperat$3 nonoperatable inoperat$3 inoperatable) near5 output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 19:03
S635	39	(latch flipflop FF ff register) same (select$3 multiplex$3 demultiplex$3 de-multiplex$3 mux$3 demux$3 de-mux$3) same (non-active nonactive inactive passiv$5 off non-operat$3 non-operatable nonoperat$3 nonoperatable inoperat$3 inoperatable) near10 output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 19:12